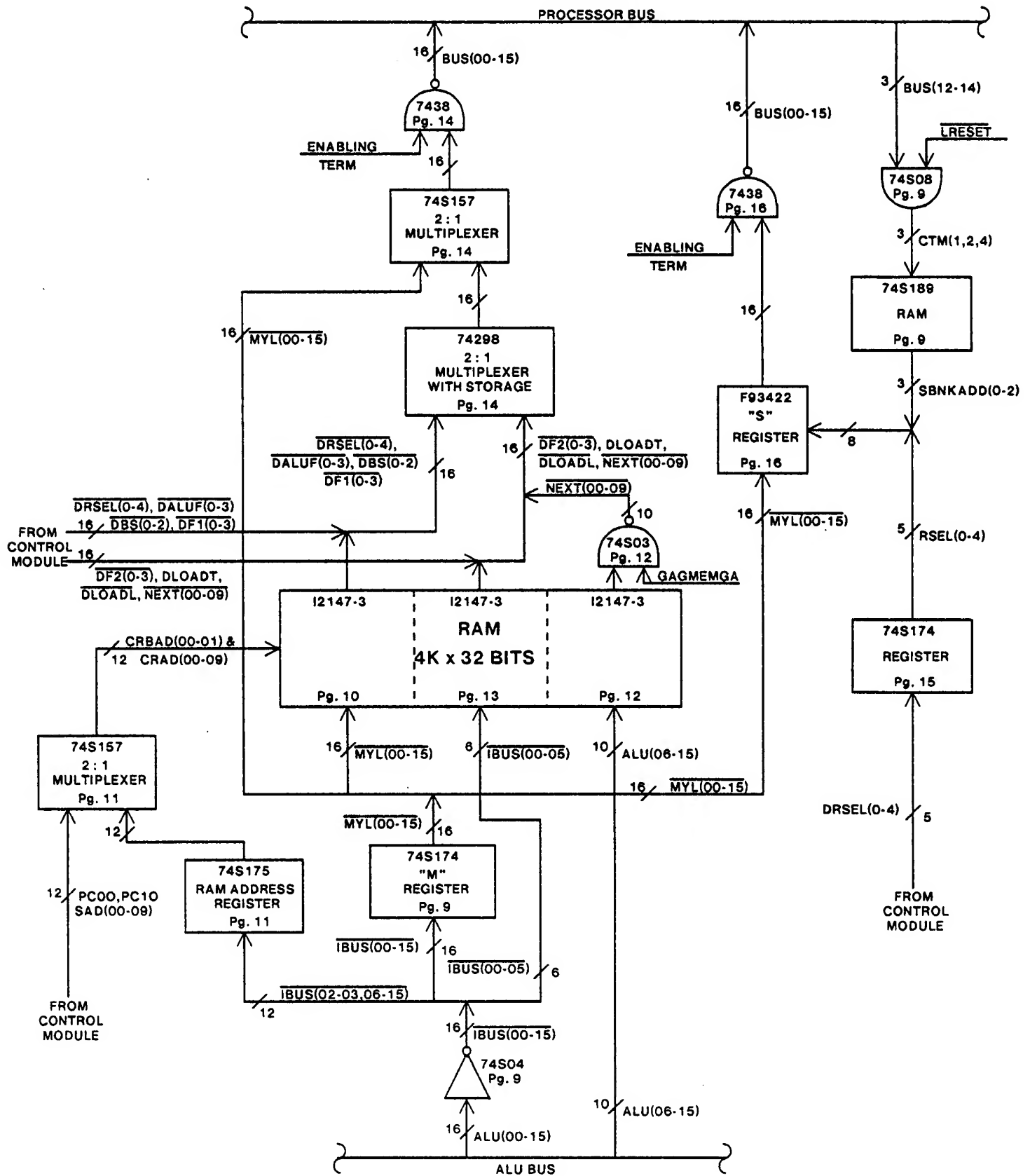## 3K CONTROL RAM

The 3K Control Ram is a standard logic card containing a fast (90 nsec.) 3072-word by 32-bit read/write microinstruction memory, 8 banks of even faster (40 nsec.) 32-word by 16-bit read/write memory (S registers), and logic to interface those memories to the Alto's microinstruction bus, processor bus, and ALU output. Unlike other microinstruction memories in the Alto, the larger memory of the 3K Control Ram can hold microinstructions and/or data.

## RAM-RELATED TASKS

The 3K Control Ram performs data manipulation (as distinct from microcode fetching) functions in response to the microinstruction. Not all tasks are likely to be interested in these functions. Moreover, not all tasks will have the appropriate values for the microinstruction uncommitted. A Ram-related task is defined as one during whose execution the 3K Control Ram card will respond to microinstructions. The standard Alto is wired so that the CPU emulator task is the only Ram-related task.

# EXTENDED MEMORY 3K CONTROL RAM MODULE
## (3KCRAM)(XM)

PROCESSOR BUS

16 / BUS(00-15)

3 / BUS(12-14)

16 / BUS(00-15)

**7438** Pg. 14

ENABLING TERM

16

16 / BUS(00-15)

LRESET

**74S08** Pg. 9

**74S157** 2 : 1 MULTIPLEXER Pg. 14

3 / CTM(1,2,4)

**7438** Pg. 16

16 / MYL(00-15)

16

ENABLING TERM

**74S189** RAM Pg. 9

**74298** 2 : 1 MULTIPLEXER WITH STORAGE Pg. 14

16

16 / DF2(0-3), DLOADT, DLOADL, NEXT(00-09)

$\overline{DRSEL(0-4)}$, $\overline{DALUF(0-3)}$, $\overline{DBS(0-2)}$ $\overline{DF1(0-3)}$

$\overline{DRSEL(0-4)}$, $\overline{DALUF(0-3)}$ 16 / $\overline{DBS(0-2)}$, $\overline{DF1(0-3)}$

**FROM CONTROL MODULE**

16

$\overline{DF2(0-3)}$, DLOADT, $\overline{DLOADL}$, NEXT(00-09)

16

$\overline{NEXT(00-09)}$

10

**74S03** Pg. 12

GAGMEMGA

**F93422** "S" REGISTER Pg. 16

8

3 / SBNKADD(0-2)

16 / MYL(00-15)

5 / RSEL(0-4)

I2147-3      I2147-3      I2147-3

**RAM** **4K x 32 BITS**

Pg. 10      Pg. 13      Pg. 12

CRBAD(00-01) & 12 CRAD(00-09)

**74S174** REGISTER Pg. 15

**74S157** 2 : 1 MULTIPLEXER Pg. 11

16 / $\overline{MYL(00-15)}$

6 / $\overline{IBUS(00-05)}$

10 / ALU(06-15)

16 / $\overline{MYL(00-15)}$

12

$\overline{MYL(00-15)}$ /16

**74S174** "M" REGISTER Pg. 9

DRSEL(0-4) / 5

**74S175** RAM ADDRESS REGISTER Pg. 11

12 / PC00,PC10 SAD(00-09)

$\overline{IBUS(00-15)}$ / 16

$\overline{IBUS(00-05)}$ / 6

$\overline{IBUS(02-03,06-15)}$ /12

**FROM CONTROL MODULE**

16 / IBUS(00-15)

**FROM CONTROL MODULE**

**74S04** Pg. 9

10 / ALU(06-15)

16 / ALU(00-15)

**ALU BUS**

NOTE: UNLESS OTHERWISE SPECFIED.
1. ASSEMBLE PER ALTO II MODULE ASSY. SPEC. DWG NO. 216207
2. PROGRAMMING THE PROMS:

   A. PROGRAM THE PROMS BEFORE IT IS INSERTED INTO THE MODULE.

   B. LABEL EACH PROM AS DEFINED AS SHOWN BELOW USING AVERY SELF-ADHESIVE (1/16X1/2)LAVEL. STICK THE LABEL ON THE TOP OF THE PROM(IC).

   C. PROGRAM THE FOLLOWING PROMS:

| PROM LABEL | LOCATION | FILE NAME | FILE LOCATION |
|---|---|---|---|
| R21B | A37 | R21B.MB | [ISIS]<SPGDOCS>PROMS>3KCRAM.DM |

   D. ADDITIONAL PROGRAM REQUIREMENT:
         a. PNEW.RUN...............[ISIS]<SPGDOCS>PROLOG.PRESS.

   E. HARDWARE REQUIREMENTS:
         a. PROLOG PROGRAMMER..........[ISIS]<SPGDOCS>PROLOG.PRESS
         b. 82S126 PROLOG PERSONALITY CARD.

3. THE FOLLOWING MODIFICATION ARE REQUIRED USING "B" REV PW BOARD ONLY. CUT ETCH PER INSTRUCTION:

   A. CUT ALL ETCH LEADING TO

   | | | | |
   |---|---|---|---|
   | A52-11 | ONE | CUT | (ETCH SIDE) |
   | A49-11 | TWO | CUTS | (ETCH SIDE) |
   | A50-11 | TWO | CUTS | (ETCH SIDE) |
   | A62-11 | TWO | CUTS | (COMP & ETCH) |
   | A63-11 | TWO | CUTS | (COMP & ETCH) |
   | A65-11 | TWO | CUTS | (COMP & ETCH) |
   | A75-11 | TWO | CUTS | (COMP & ETCH) |
   | A78-11 | TWO | CUTS | (ETCH SIDE) |
   | A88-11 | TWO | CUTS | (COMP. SIDE) |
   | A91-11 | TWO | CUTS | (ETCH SIDE) |
   | A61-15 | ONE | CUTS | (COMP. SIDE) |

   CUT ALL ETCH LEADING TO    A25-1    ONE   CUT    (ETCH SIDE)

   B. CUT BOTH ETCH TO FEEDTHROW    BETWEEN A68-18 AND A69-1 (ETCH,COMP    )
   C. CUT ETCH TO FEED THROUGH BETWEEN A52-10 AND A53-9 (COMP SIDE)
   D CUT ETCH TO EDGE CONNECTOR FINGER    J2-13 (ETCH SIDE)
   E. CUT ETCH TO EDGE CONNECTOR FINGER    J2-15   (ETCH SIDE)
   F. CUT ETCH TO EDGE CONNECTOR FINGER    J2-29   (ETCH SIDE)
   G. CUT ETCH TO EDGE CONNECTOR FINGER    J2-30   (ETCH SIDE)
   H. CUT ETCH TO A84-1 (COMP SIDE)

4. THE FOLLOWING MODIFICATION ARE REQUIRED USING "B" REV PW BOARD ONLY. ADD JUMPER PER INSTRUCTION

   | | | | | | |
   |---|---|---|---|---|---|
   | A. ADD JUMPER FROM | P2-12 | TO | A70-9 | (ETCH SIDE) | |
   | B. ADD JUMPER FROM | P2-13 | TO | A90-9 | (ETCH SIDE) | GND |
   | C. ADD JUMPER FROM | P2-15 | TO | A91-9 | (ETCH SIDE) | GND |
   | D. ADD JUMPER FROM | P2-29 | TO | A92-9 | (ETCH SIDE) | GND |
   | E. ADD JUMPER FROM | P2-30 | TO | A93-9 | (ETCH SIDE) | GND |

FILE: 3KCRAM02.SIL

| TITLE | | DWG. SIZE | DWG. NO. | | SHEET REV. |
|---|---|---|---|---|---|
| ASSEMBLY, P.W. | | | 217812 | | |
| 3K CRAM MODULE | | A4 | SHEET OF 2 | 17 | E |

4. THE FOLLOWING MODIFICATIONS ARE REQUIRED USING "B" REV PW BOARD ONLY.
   ADD JUMPER PER INSTRUCTION:

   a.  A49-11 TO A23-5
       A62-11 TO A23-3
       A75-11 TO A23-1
       A88-11 TO A12-1
       A50-11 TO A12-3
       A52-11 TO A23-9
       A63-11 TO A12-5
       A65-11 TO A23-11
       A78-11 TO A23-13
       A91-11 TO A12-13
       A21-15 TO A21-8
       A24-13 TO A25-1
       A87-15 TO A87-8
       A66-11 TO A35-7
       A57-1  TO P1-69
       A57-2  TO  A39-1
       A57-3 TO  A61-15
       A45-4 TO A12-9
       A12-8 TO FEED THROUGH BETWEEN A52-10 AND A53-9

FILE:  3KCRAM03.SIL

TITLE

ASSEMBLY, P.W.
3K CRAM MODULE

DWG. SIZE

A4

DWG. NO.  218812

SHEET 3    OF    18

SHEET REV.

E

NOTE: THE FOLLOWING MODIFICATION INSTRUCTION(5,6,&7) SHOULD BE DONE ON
"B" REV PWB ONLY.

5.0 DRILL HOLE:      a. DRILL HOLE PER FIGURE3.

6.0 MOUNT CABLE ASSEMBLY (2533)AND PLATE ASSEMBLY (218054-001) PER
FIG. 1 AND FIG.2.

7.0 ADD WIRE (OBSERVE FIGURE 4)

| | | |
|---|---|---|
| CONDUCTOR 1 TO A83-07 | GND | CIRCUIT SIDE |
| CONDUCTOR 2 TO A84-08 | GND | CIRCUIT SIDE |
| CONDUCTOR 7 TO A84-13 | CT8 | CIRCUIT SIDE |
| CONDUCTOR 8 TO A84-14 | CT4 | CIRCUIT SIDE |
| CONDUCTOR 9 TO A84-15 | CT3 | CIRCUIT SIDE |
| CONDUCTOR 10 TO A84-01 | CT1 | CIRCUIT SIDE |

PLATE
218054-001
218054-002

CIRCUIT SIDE

FIG. 1

COMP.
SIDE

ETCH
SIDE

PLATE      PLATE

FIG. 2

0.95"      1.50"

X      X

DRILL HOLE
0.120 INCHES
DIAMETER

CIRCUIT SIDE

FIG. 3

TO A83-07    CONDUCTOR1           RED         1
TO A84-08    CONDUCTOR2
TO A84-13    CONDUCTOR 7
TO A84-14    CONDUCTOR8
TO A84-15    CONDUCTOR9
TO A84-01    CONDUCTOR10
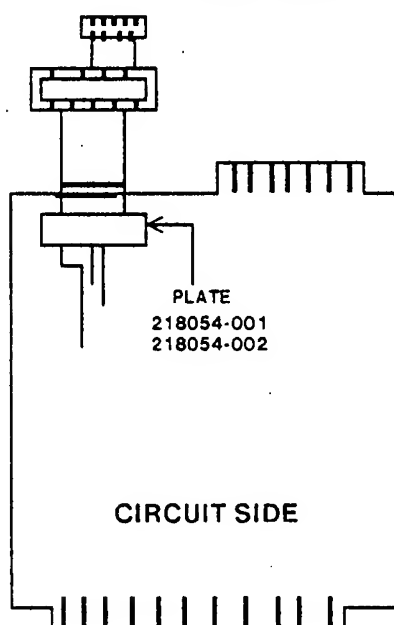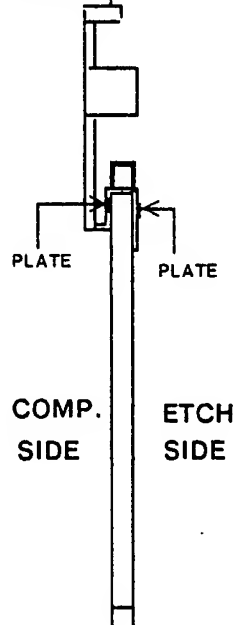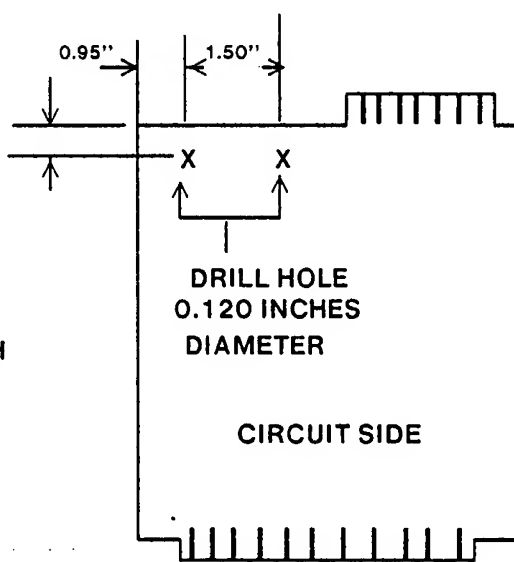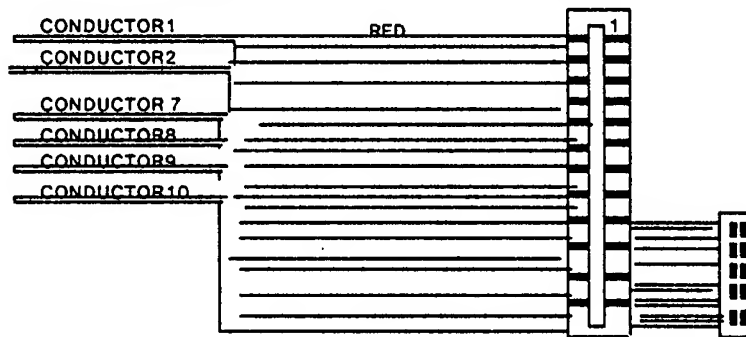
FIG. 4

8.0 THE FOLLOWING MODIFICATION INSTRUCTIONS SHOULD BE DONE ON
"C" REV PWB ONLY

* CUT ETCH LEADING TO A25-1          2 CUTS ON COMPONENT SIDE

* ADD WIRE: A25-1 TO A24-13
A38-1 TO A1-09

FILE:  3KCRAMO4.SIL

| TITLE | | DWG. SIZE | DWG. NO. 217812 | | | SHEET REV. |
|---|---|---|---|---|---|---|
| ASSEMBLY, P.W. | | | | | | |
| 3K CRAM MODULE | | A4 | SHEET 4 | OF | 17 | E |

13

14

2 PLACES

50 J2 2 26 J3 R10 2

R5 R7

A95 A94 A93 A92 A91 A90 A89 A88 A87 A86 A85 A84 A83

—C50— —C49— —C48— —C47— —C46— —C45— —C44—

A82 A81 A80 A79 A78 A77 A76 A75 A74 A73 A72 A71 A70

—C43— —C42— —C41— —C40— —C39— —C38— R4 —C37—
R9

A69 A68 A67 A66 A65 A64 A63 A62 A61 A60 A59 A58 A57

—C36— —C35— —C34— —C33— —C32— —C31— A101 —C30—

A56 A55 A54 A53 A52 A51 A50 A49 A48 A47 A46 A45

—C29— —C28— —C27— —C26— —C25— R3 —C24— —C23—

A44 A43 A42 A41 A40 A39 A38 A37 A36

—C51— —C22— —C21— —C20—
A100

A35 A34 A33 A32 A31 A30 A29 A28 A27 A26 A25 A24

—C18—
—C19— —C16— —C15— —C14—

A99 A98 A97

A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13

—C13— —C12— —C11— —C8—
—C10— —C9—

A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1

—C7— —C6— —C5— R1 —C1—
R8 CR1
R6 C2 A96

12

61 1

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

FILE: 3KCRAM07.SIL

TITLE ASSEMBLY, P.W.
3K CRAM MODULE

DWG. SIZE
A4

DWG. NO. 217812

SHEET 7 OF 17

SHEET REV.
E

ALU(00) 5 S04 6 a11c IBUS(00)'
ALU(01) 3 S04 4 a11b IBUS(01)'
ALU(02) 1 S04 2 a11a IBUS(02)'
ALU(03) 9 S04 8 a11d IBUS(03)'
ALU(04) 11 S04 10 a11e IBUS(04)'
ALU(05) 13 S04 12 a11f IBUS(05)'

101
102
103
104
105

S174
3 D0 Q0 2 MYL(00)'
4 D1 Q1 5 MYL(01)'
6 D2 Q2 7 MYL(02)'
11 D3 Q3 10 MYL(03)'
13 D4 Q4 12 MYL(04)'
14 D5 Q5 15 MYL(05)'
9 CK CL' 1 a22

ALU(06) 5 S04 6 a12c IBUS(06)'
ALU(07) 3 S04 4 a12b IBUS(07)'
ALU(08) 1 S04 2 a12a IBUS(08)'
ALU(09) 1 S04 2 a23a IBUS(09)'
ALU(10) 3 S04 4 a23b IBUS(10)'
ALU(11) 5 S04 6 a23c IBUS(11)'

106
107
108
109
110
111

S174
3 D0 Q0 2 MYL(06)'
4 D1 Q1 5 MYL(07)'
6 D2 Q2 7 MYL(08)'
11 D3 Q3 10 MYL(09)'
13 D4 Q4 12 MYL(10)'
14 D5 Q5 15 MYL(11)'
9 CK CL' 1 a34

ALU(12) 13 S04 12 a12f IBUS(12)'
ALU(13) 13 S04 12 a23f IBUS(13)'
ALU(14) 11 S04 10 a23e IBUS(14)'
ALU(15) 9 S04 8 a23d IBUS(15)'

112
113
114
115

S174
3 D0 Q0 2 MYL(12)'
4 D1 Q1 5 MYL(13)'
6 D2 Q2 7 MYL(14)'
11 D3 Q3 10 MYL(15)'
13 D4 Q4 12
14 D5 Q5 15
9 CK CL' 1 a35

pr

SysClk 12
LoadL 10
GoodTask 9 H20 8
13 a24c
pr

J3-10 CT1
J3-09 CT2
J3-08 CT4
J3-07 CT8

bus(12) 13 / 12 S08 11 a83d
bus(13) 5 / 4 S08 6 a83b
bus(14) 10 / 9 S08 8 a83c
bus(15) 2 / 1 S08 3 a83a
LReset'

A0 S189
15 A1
14 A2
13 A3
4 D0 Q0' 5 CT1M'
6 D1 Q1' 7 CT2M'
10 D2 Q2' 9 CT4M'
12 D3 Q3' 11 CT8M'
CS' WE' a84
2 3

DbSysClk'

S175
4 D0 Q0 3 SBNKADD0
Q0' 7
5 D1 Q1 6 SBNKADD1
Q1' 10
12 D2 Q2 11 SBNKADD2
Q2' 15
13 D3 Q3 14 SBNKADD3
Q3'
CK CL' a71
9 1 pr

EmAct 1 A S138
F1(2)' 2 B
F1(1)' 3 C
Y0'
Y1'
Y2'
Y3' 12
Y4' 11
F1(0):R 6 EN Y5' 10
(3)' 4 GA Y6'
GoodTask' 5 GB Y7'
a38

3 / 4 / 5 S10 6 a40b
9 S04 8 a58d SRegBankEn'

ClkModeS'

| XEROX ED | Project 3K CRAM | ALU INTERFACE TASK CONTROL | File 3KCRAM09.SIL | Designer ALBERT PAE | Rev E | Date 2/21/79 | Page 9 |

## Chip a93 (I2147)
MYL(00)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'  10  8
RAMCS'
DWE'

## Chip a80 (I2147)
MYL(01)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a67 (I2147)
MYL(02)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a54 (I2147)
MYL(03)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

DRSel0'  44  <P2-39
DRSel1'  46  <P2-40
DRSel2'  47  <P2-41
DRSel3'  48  <P2-42

## Chip a94 (I2147)
MYL(04)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'
RAMCS'
DWE'

## Chip a81 (I2147)
MYL(05)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a68 (I2147)
MYL(06)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a55 (I2147)
MYL(07)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

DRSel4'  49  <P2-43
DALUF0'  50  <P2-44
DALUF1'  51  <P2-45
DALUF2'  52  <P2-46

## Chip a95 (I2147)
MYL(08)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'
RAMCS'
DWE'

## Chip a82 (I2147)
MYL(09)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a69 (I2147)
MYL(10)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a56 (I2147)
MYL(11)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

DALUF3'  57  <P2-47
DBS0'  54  <P2-48
DBS1'  55  <P2-49
DBS2'  56  <P2-50

## Chip a92 (I2147)
MYL(12)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'
RAMCS'
DWE'

## Chip a79 (I2147)
MYL(13)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a66 (I2147)
MYL(14)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

## Chip a53 (I2147)
MYL(15)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
DO 7
CS' WE'

DF1(0)  40  <P2-36
DF1(1)'  41  <P2-35
DF1(2)'  42  <P2-38
DF1(3)'  43  <P2-37

XEROX ED — Project: 3K CRAM — ADDRESS SELECT — File: 3KCRAM11.SIL — Designer: ALBERT PAE — Rev: E — Date: 2/17/79 — Page: 11

**Block a63 (I2147)**
ALU(06) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a63
10 8
DWE'

**Block a50 (I2147)**
ALU(07) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a50
10 8

**Block a88 (I2147)**
ALU(08) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a88
10 8

**Gates (top)**
4, 5 → SO3 6 a43b → Next(00)' 23 — P2-19
1, 2 → SO3 3 a43a → Next(01)' 24 — P2-20
2, 1 → SO3 3 a42a → next(02)' 25 — P2-21

**Block a75 (I2147)**
ALU(09) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a75
10 8
DWE'

**Block a62 (I2147)**
ALU(10) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a62
10 8

**Block a49 (I2147)**
ALU(11) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a49
10 8

**Gates (middle)**
5, 4 → SO3 6 a42b → Next(03)' 26 — P2-22
12, 13 → SO3 11 a42d → Next(04)' 28 — P2-23
9, 10 → SO3 8 a42c → Next(05)' 116 — P2-24

**Block a91 (I2147)**
ALU(12) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
-CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a91
10 8
DWE'

**Block a78 (I2147)**
ALU(13) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a78
10 8

**Block a65 (I2147)**
ALU(14) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a65
10 8

**Gates (lower)**
5, 4 → SO3 6 a44b → Next(06)' 117 — P2-25
9, 10 → SO3 8 a44c → Next(07)' 118 — P2-26
1, 2 → SO3 3 a44a → Next(08)' 119 — P2-27

**Block a52 (I2147)**
ALU(15) 11 DI
CRBAD(00) 1 A0
CRBAD(01) 2 A1
CRAD(00) 3 A2
CRAD(01) 4 A3
CRAD(02) 5 A4
CRAD(03) 6 A5
CRAD(04) 17 A6
CRAD(05) 16 A7
CRAD(06) 15 A8
CRAD(07) 14 A9
CRAD(08) 13 A10
CRAD(09) 12 A11
DO 7
CS' WE' a52
10 8
DWE'
GagMemGa

**Gate (bottom)**
12, 13 → SO3 11 a44d → Next(09)' 120 — P2-28

**Chip a90 (I2147):**

IBUS(00)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7    DO 7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
CS' WE' a90

**Chip a77 (I2147):**

IBUS(01)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7    DO 7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
CS' WE' a77

**Chip a64 (I2147):**

IBUS(02)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7    DO 7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
CS' WE' a64

**Chip a51 (I2147):**

IBUS(03)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7    DO 7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
CS' WE' a51

RAMCS'
DWE'

DF2(0)  [33]
<P2-32

DF2(1)'  [36]
<P2-31

DF2(2)'  [37]
<P2-34

DF2(3)'  [38]
<P2-33

**Chip a89 (I2147):**

IBUS(04)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7    DO 7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
RAD(08) 13 — A10
RAD(09) 12 — A11
CS' WE' a89

**Chip a76 (I2147):**

IBUS(05)' 11 — DI
CRBAD(00) 1 — A0
CRBAD(01) 2 — A1
CRAD(00) 3 — A2
CRAD(01) 4 — A3
CRAD(02) 5 — A4
CRAD(03) 6 — A5
CRAD(04) 17 — A6
CRAD(05) 16 — A7    DO 7
CRAD(06) 15 — A8
CRAD(07) 14 — A9
CRAD(08) 13 — A10
CRAD(09) 12 — A11
CS' WE' a76

RAMCS'
DWE'

DLoadT'  [31]
<P2-18

DLoadL  [30]
<P2-17

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|---|---|---|---|---|---|---|---|---|
| ED | 3K CRAM | S REGISTER CONTROL | 3KCRAM15.SIL | | ALBERT PAE | E | 2/17/79 | 15 |

RdRegS 2
LRef' 5
Const' 1
GoodTask 4
H21 6
a27c
pr

F93422
SBNKADD0 4 A0
SBNKADD1 3 A1 Q0 10
SBNKADD2 2 A2
RSel0' 1 A3
RSel1' 21 A4
RSel2' 5 A5 Q1 12
RSel3' 6 A6
RSel4' 7 A7
Q2 14
MYL(00)' 9 D0
MYL(01)' 11 D1
MYL(02)' 13 D2 a15 Q3 16
MYL(03)' 15 D3
RWE 20 WE' C' CS OE' 18
19 17
SBNKADD3 pr

pr 1 2 38 3 BUS(00) 80 a4a
pr 4 5 38 6 BUS(01) 81 a4b
pr 13 12 38 11 BUS(02) 82 a4c
pr 10 9 38 8 BUS(03) 83 a4d

F93422
SBNKADD0 4 A0
SBNKADD1 3 A1 Q0 10
SBNKADD2 2 A2
RSel0' 1 A3
RSel1' 21 A4
RSel2' 5 A5 Q1 12
RSel3' 6 A6
RSel4' 7 A7
Q2 14
MYL(04)' 9 D0
MYL(05)' 11 D1
MYL(06)' 13 D2 a16 Q3 16
MYL(07)' 15 D3
RWE 20 WE' C' CS OE' 18
19 17
SBNKADD3 pr

pr 2 1 38 3 BUS(04) 84 a5a
pr 4 5 38 6 BUS(05) 85 a5b
pr 12 13 38 11 BUS(06) 86 a5c
pr 10 9 38 8 BUS(07) 87 a5d

F93422
SBNKADD0 4 A0
SBNKADD1 3 A1 Q0 10
SBNKADD2 2 A2
RSel0' 1 A3
RSel1' 21 A4
RSel2' 5 A5 Q1 12
RSel3' 6 A6
RSel4' 7 A7
Q2 14
MYL(08)' 9 D0
MYL(09)' 11 D1
MYL(10)' 13 D2 a17 Q3 16
MYL(11)' 15 D3
RWE 20 WE' C' CS OE' 18
19 17
SBNKADD3 pr

pr 2 1 38 3 BUS(08) 88 a6a
pr 5 4 38 6 BUS(09) 89 a6b
pr 10 9 38 8 BUS(10) 90 a6c
pr 13 12 38 11 BUS(11) 91 a6d

F93422
SBNKADD0 4 A0
SBNKADD1 3 A1 Q0 10
SBNKADD2 2 A2
RSel0' 1 A3
RSel1' 21 A4
RSel2' 5 A5 Q1 12
RSel3' 6 A6
RSel4' 7 A7
Q2 14
MYL(12)' 9 D0
MYL(13)' 11 D1
MYL(14)' 13 D2 a14 Q3 16
MYL(15)' 15 D3
RWE 20 WE' C' CS OE' 18
19 17
SBNKADD3 pr

pr 1 2 38 3 BUS(12) 92 a3a
pr 10 9 38 8 BUS(13) 93 a3c
pr 13 12 38 11 BUS(14) 94 a3d
pr 4 5 38 6 BUS(15) 95 a3b

RdRegS 12
LRef' 9
Const' 13
GoodTask 10
H21 8
a27c
pr

IBUS(00)'
IBUS(02)'
IBUS(04)'
IBUS(06)'
IBUS(08)'
IBUS(10)'
IBUS(12)'
IBUS(14)'

N166

A
B
C
D
E
F
G
H

QH 13

SI
SL

CK CL' CE'  a85
7  9  6

DbSysCk'
OKToRun
DoModeS'
ClkModeS'

pr
pr

pr

X0 S153
X1
X2
X3

Y0
Y1
Y2
Y3

S2
S1
EX'  EY'  a59

6
5
4
3

10
11
12
13

2
14
1  15

OX 7

OY 9

ModeSH

DoModeS'

71

IBUS(01)'
IBUS(03)'
IBUS(05)'
IBUS(07)'
IBUS(09)'
IBUS(11)'
IBUS(13)'
IBUS(15)'

N166

A
B
C
D
E
F
G
H

QH 13

SI
SL

CK CL' CE'  a72
7  9  6

LReset
Next(09)'

10
9

H00
a46c

8 13

S04
a58f

12